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EXAMINER	
PLANTE, JONATHAN R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,103	SMITH ET AL.	
	Examiner	Art Unit	
	Jonathan R. Plante	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *1-7 and 14-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application Number: 10/812,103 has a total of 6 claims pending in the application; there is 1 independent claim and 5 dependent claims, all of which are ready for examination by the examiner.

Examiner acknowledges receipt of "Amendments to the Claims" received on 30 March 2004. Applicant has canceled claims 1-7 and claims 14-15 and for purpose of this examination claim 1-7, and 14-15 will not be evaluated. Claims pending in the application are the originally numbered claims 8-13.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

Drawings

3. The drawings are objected to because of failure by applicant to:

a. Number/index the figures appropriately,

b. Replace "**FIG. 1 (State of the Art)**" with "FIG. 1 (Prior Art)",

c. All labels and titles should be in type text not hand written.

Applicant is requested to review the Manual of Patent Examining Procedure (MPEP) Section 608.02 – Drawing for further clarification on drawing requirements.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.

(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.

(f) BACKGROUND OF THE INVENTION.

(1) Field of the Invention.

(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(g) BRIEF SUMMARY OF THE INVENTION.

(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

(i) DETAILED DESCRIPTION OF THE INVENTION.

(j) CLAIM OR CLAIMS (commencing on a separate sheet).

(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

In review of the application specification the examiner is objecting to the submitted format as not conforming to the requirements outlined above as (f) – (i). The examined specification contains a background section, followed by three embodiments, followed by brief description of the drawings, then the preferred embodiment, and last a physical structure description. The current specification is missing a specific detailed description of the invention. Applicant is requested in response to this correspondence to submit a properly formatted specification that conforms to the above 37 CFR 1.77(b). Applicant is cautioned about adding new subject matter.

Specification Objections

5. The specification is objected to because of the following informalities:

a. Applicant is cautioned that the specification is to be written in narrative form, and that claim grammatical language/syntax is to be avoided. Specifically the applicant has presented multiple embodiments of the invention in the specification written in claim structure (Page 3, Lines 4-20) (Page 4, Lines 1-17) and (Page 5, Lines 1-14).

b. Please replace "**relates to**" (Page 1, Line 7) with "relates to an".

c. Please replace "**system for**" (Page 1, Line 8) with "system for the".

d. Please remove paragraph 3 (Page 2, Line 8-10), block instantiation is not applicable to application.

e. Please replace "**example for**" (Page 2, Line 13) with "example of".

f. Please replace "**NCVerilog**" (Page 2, Line 14) with "NCVerilog ®".

g. Please remove "**available from**" (Page 2, Line 14).

h. Please replace "**Cadence**" (Page 2, Line 14) with "(Cadence".

i. Please replace "**95134.**" (Page 2, Line 15) with "95134)."

j. Please replace "**"cycle level". Simulation comprises basically a**" (Page 2, Line 17) with " "cycle level" simulation that comprises of a".

k. Please replace "**In cycle level simulations**" (Page 2, Line 19) with "In "cycle level" simulations".

l. Please replace "**to find**" (Page 3, Line 5) with "for the finding of".

m. Please replace "**the invention,**" (Page 3, Line 7) with "the invention is".

n. Please replace "**for simulation**" (Page 3, Line 7) with "for the simulation".

o. Please replace "**circuit is provided, the**" (Page 3, Line 8) with "circuit. The"

p. Please replace "**elements, the**" (Page 3, Line 9) with "elements. The".

q. Please replace "**comprising first and second asynchronous**" (Page 3, Line 9) with "comprising of a first and of a second (asynchronous)".

r. Please replace "**portions of circuit**" (Page 3, Line 10) with "portions of the circuit".

s. Please replace "**first and second**" (Page 3, Line 11) with "first and the second".

t. Please replace "**domains, the**" (Page 3, Line 11) with "domains. The".

u. Please remove "**Preferably**" (Page 3, Line 13).

v. Please replace "**may be**" (Page 3, Line 13) with "can".

w. Please replace "**on cycle level of a description**" (Page 3, Line 13) with "on a "cycle level" description".

x. Please remove "**Preferably**" (Page 3, Line 15).

y. Please replace "**may**" (Page 3, Line 15) with "can".

z. Please replace "**comprise delay**" (Page 3, Line 15) with "comprise of delay".

aa. Please remove "**Further preferably**" (Page 3, Line 17).

bb. Please replace "**may**" (Page 3, Line 17) with "can".

cc. Please replace "**comprise x generator**" (Page 3, Line 17) with "comprise of x generator".

dd. Please remove "**Yet further preferably**" (Page 3, Line 19).

ee. Please replace "**may**" (Page 3, Line 19) with "can".

ff. Please replace "**provides a**" (Page 4, Line 4) with "provides for a".

gg. Please replace "**circuit, the**" (Page 4, Line 5) with "circuit. The".

hh. Please replace "**elements, the**" (Page 4, Line 6) with "elements. The".

ii. Please replace "**comprising first and second asynchronous**" (Page 4, Line 6) with "comprising of a first and of a second (asynchronous)".

jj. Please replace "**first and second**" (Page 4, Line 8) with "first and the second".

kk. Please replace "**domains, the**" (Page 4, Line 8) with "domains. The"

ll. Please remove "**Preferably**" (Page 4, Line 10).

mm. Please replace "**may**" (Page 4, Line 10) with "can".

nn. Please replace "**on cycle level of a description**" (Page 4, Line 10) with "on a "cycle level" description".

oo. Please remove "**Preferably**" (Page 4, Line 12).

pp. Please replace "**may**" (Page 4, Line 12) with "can".

qq. Please replace "**comprise delay**" (Page 4, Line 12) with "comprise of delay".

rr. Please replace "**is**" (Page 4, Line 13) with "are".

ss. Please remove "**Further preferably**" (Page 4, Line 14).

tt. Please replace "**may**" (Page 4, Line 14) with "can".

uu. Please replace "**comprise x generator**" (Page 4, Line 14) with "comprise of x generator".

vv. Please remove "**Yet further preferably**" (Page 4, Line 17).

ww. Please replace "**may**" (Page 4, Line 17) with "can".

xx. Please replace "**at cycle level**" (Page 5, Line 9) with "at the cycle level simulation".

yy. Please replace "**gate level.**" (Page 5, Line 10) with "gate level simulation.".

zz. Please replace "**in a computer**" (Page 5, Line 13) with "in computer".

aaa. Please replace "**need**" (Page 5, Line 13) with "used".

bbb. Please replace "**comprise several portions**" (Page 6, Line 8) with "comprise of several partitions"

ccc. Please replace "**clocks.**" (Page 5, Line 9) with "clocks (asynchronous)".

ddd. Please replace "**portions**" (Page 5, Line 10) with "partitions"

eee. Please replace "**from 0 to 3**" (Page 6, Line 16) with "from a 0 to a 3".

fff. Please replace "**portions**" (Page 6, Line 19) with "partitions".

ggg. Please define "**probability of meter stability**" (Page 7, Line 1). Please provide prior art documentation defining "probability of meter stability".

hhh. Please replace "**data are handed over**" (Page 7, Line 15) with "data is crossing".

iii. Please insert "**(ASIC)**" (Page 9, Line 9) after "integrated circuits".

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification. Appropriate correction is required.

Claim Objections

6. Claims 8, 9, and 10 are objected to because of the following informalities:

a. Please replace "**comprising first and second**" (Claim 8, Line 2) with "comprising of a first and of a second".

b. Please replace "**the first and second**" (Claim 8, Line 4) with "the first and the second" for clarification.

c. Please replace "**out on cycle level of a description**" (Claim 9, Line 1) with "out on a cycle level description" for clarification.

d. Please replace "**which is**" (Claim 10, Line 2) with "which are".

Appropriate correction is required.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 9-13 are rejected under 35 U.S.C. 101 because they fail to produce (claim) a real-world result. Claims 9-13 relate to a process of simulating an electronic circuit, however the claimed process does not produce (claim) a real-world result that is useful, tangible, and concrete.

In determining whether the claim is for a "practical application," the focus is not on whether the steps taken to achieve a particular result are useful, tangible, and concrete, but rather that the final result achieved by the claimed invention is "useful, tangible, and concrete." In the instant application claims 9-13, the mere simulation of a system does not produce a "useful, tangible, and concrete" result, and the applicant has not claimed a final result that is "useful, tangible, and concrete" outside of the simulation steps (process) its self.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claims 8, 9, 12, and 13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As per claim 8, the applicant is claiming a simulation system for the simulation of an electronic system, but the applicant has failed to disclose in the instance application a written description of the simulation system that would enable any person skilled in the art to reproduce the instant simulation technique. The applicant has provided a generic structural/hardware description (Pages 8 -10) inclusive of any computer system consisting of a processor, memory, software, and input/output devices. The specification fails to disclose to one skilled in the art how the simulation system is structured in reference to:

a. What data is provided to the simulation?

b. How is the data provided to the system?

c. What is the system simulating (i.e. logic/timing/delay)?

d. What criteria/algorithm is the simulation using to evaluate the simulation?

e. How are the results interpreted by the simulation?

f. How are the simulation result outputted/displayed?

As per claim 9, the applicant claims, "the simulation is carried out on a cycle level of a description" (Claim 9, Line 1), and according to the specification "In cycle level simulations logic functions effectively happen in zero time, so generally all signals appear to change at the same time." (Page 2, Line 19). Claim 9 is rejected for the failure of the applicant to disclose to one skilled in the art how a "cycle level" description/simulation accounts for the "jitter elements" (Claim 8, Line 3) defined as "Jitter elements according to the invention comprise delay elements and x generator elements" (Page 7, Line 5) in the simulation. The application and review of the prior art define a "cycle level" simulation, as a simulation that does not account for timing, slew, and/or logic delay meaning that a "cycle level" simulation only evaluates the functional status of the circuit. As a result the applicant has claimed the application of a "cycle level" simulation with the application of timing delay elements, but has failed to disclose how the "cycle level" simulation has been modified to account for timing. The usage of a non-timing simulation technique it at opposition with the application of added elements for the purpose of increasing the time delays.

For purpose of this office action the examiner will interpret the "cycle level" simulation to be defined as "Cycle based simulations allow the designer to examine the results at the end of a cycle. A cycle based simulator does not have to determine the propagation delay of the logic elements in the design." Vaidyanathan et al. (US 5,809,283) (Column 2, Line 4), and for the evaluation of claims relating to the application of timing delay a "event-driven" simulation will be applied and defined as "Event-driven simulators propagate signals from the output of one system element to

the inputs of the next system element and allow the designer to examine the results of the propagation throughout a clock cycle. Additionally, the event-driven simulators simulate the propagation delay of the logic elements in the design." Vaidyanathan et al. (US 5,809,283) (Column 1, Line 64). It is the opinion of the examiner that these definitions for "cycle" and "event-driven" simulations are uniform definitions for individuals skilled in the art, based on prior art and knowledge of one skilled in the art.

As per claim 12 and 13, the applicant has failed to disclose to one skilled in the art what criteria or methodology is applied in determining when an insertion or addition of "jitter elements" is to be performed on the circuit during simulation. The applicant has additionally failed to disclose what the functional result is of adding these "jitter elements" to the simulation.

Applicant is requested to specifically cite (reference) support in the specification for claims 8, 9, 12, and 13 in reference to the claims in response to this office action without the addition of new subject matter.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 8 the usage of the phrase "jitter elements" is rejected

as a result of multiple provided definitions or structures referred to as "jitter elements" in the specifications:

a. "the jitter elements may further comprise delay elements for introducing predetermined timing delays which are randomly exercised." (Page 3, Line 15)

b. "the jitter elements may also comprise x generator elements for introducing predetermined signal values which are randomly generated." (Page 3, Line 17)

For the examining the instant application it will be the examiner's interpretation for claim 8 that "jitter elements" can be either "delay elements" (Page 3, Line 15) or "x generator elements" (Page 3, Line 17).

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 8, 10, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by B. W. Curran et al. ("IBM eServer z900 high-frequency microprocessor technology, circuits, and design methodology" July/September 2002, IBM Journal of Research and Development, VOL. 46, NO 4/5).

As per claim 8, Curran et al. discloses, "the circuit being representable by a network of logical elements" as **["The random logic macro descriptions (VHDL) were**

first synthesized into gate-level netlists" (Page 638, Column 2) and **"macros with latch counts as high as 1400" (Page 639, Column 2)]** "the circuit comprising first and a second asynchronous clock domains" **["FIG. 1, CLOCK" (Page 633)** and **"FIG. 3, CLKG, CKL" (Page 634)]** "wherein jitter elements are additionally insertable at predetermined portions of circuit boundaries between the first and second clock domains" **[early-mode pad books were to be inserted at latch inputs or outputs. (Pad books are special buffer gates which incorporate non-minimum-channel-length devices.) (Page 639, Column 1)]** "the jitter elements being representable as logic elements, the values of which are randomly set" **["A new synthesis engine was built upon a continuous gate-sizing technique" (Page 638 Column 1)** and **"The new synthesis engine, which utilizes continuous optimization techniques, was able to fully exploit the enhanced four-dimensional gate library." (Page 638, Column 1)** and **"Four-dimensional RLM library" (Page 638, FIG. 7)]**.

In rejection to claim 8 the application of a synthesis system to a simulation system is appropriate based on the conclusion that the process and system of simulation is a component or sub-process of the process and system of synthesis (logic construction from functional definitions) in its entirety. Additionally the application of early-mode padding is the application of inserting logic (delay) between two or more circuit boundaries to avoid the latching (capturing) of signals early relative to clocks across the clock boundaries.

As per claim 10, Curran et al. discloses, "the jitter elements comprise delay elements for introducing predetermined timing delays which is randomly generated" as

[synthesis selected the smallest delay book that fixed the early-mode path (Page 639, Column 1)].

As per claim 13, Curran et al. discloses, "wherein the jitter elements are automatically inserted using predetermined modules." as **[early-mode problems were automatically fixed (Page 639, Column 6)]**.

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

16. Claims 8, 9, 11, and 12 are rejected under 35 U.S.C. 102(a) as being anticipated by Hoppe et al. (US 2004/0230414 A1) November 18, 2004.

17. As per claim 8, Hoppe et al. discloses, "Simulation system for simulation of an electric circuit" as **[A system and method are described herein to perform asynchronous stress testing using a single cycle random simulation environment (Abstract)]** "being represented by a network of logical elements" **[Any complex application specific integrated circuit (ASIC) design (Page 1, Paragraph 0008)]** "the circuit comprising first and second asynchronous clock domains" **[The circuit chip logic operating at multiple frequency domains (Page 2, Paragraph 0025)]** "wherein jitter elements are additionally insertable at predetermined portions of the circuit boundaries between the first and second clock domains" **["A verification engineer 44 inputs a design specification to a behavioral checker." (Page 2, Paragraph 0022)**

and **"logical problems such as, buffer underruns, buffer overruns, and protocol violations can be identified" (Page 3, Paragraph 0036)]** "the jitter elements being representable as logical elements, the value of which are randomly set" **["A verification engineer inputs a design specification to a behavioral checker." (Page 2, Paragraph 0022)** and **"The simulator exercises design in accordance with test programs, which may be generated automatically or written by engineer or other personnel." (Page 2, Paragraph 0023)** and **"the single cycle random simulation environment is normally used for all functional verification" (Page 3, Paragraph 0035)].**

As per claim 9, Hoppe et al. discloses, "wherein the simulation is carried out on cycle level of a description of the electronic circuit" **[Verification of the STI Switch chip is performed with an IBM-designed cycle simulator called ZFS. With a cycle simulator such as ZFS, the detailed timing of the logic circuits is ignored, and the state of the logic is evaluated on clock cycle boundaries." (Page 1, Paragraph 0009)].** The usage of Hoppe et al. and the application of "cycle" simulator is only applicable to the "jitter elements" defined as "x generator elements for introducing predetermined signal values" (Page 3, Line 17). The application of Hoppe et al. does not release applicant from responding to the 35 USC § 102 rejections/objections cited in this office action in relationship to a "cycle level" simulation and application of timing data.

As per claim 11, Hoppe et al. discloses, "wherein the jitter elements comprise x generator elements for introducing predetermined signal values which are randomly

generated" **["A verification engineer inputs a design specification to a behavioral checker." (Page 2, Paragraph 0022)** and **"The simulator exercises design in accordance with test programs, which may be generated automatically or written by engineer or other personnel." (Page 2, Paragraph 0023)** and **"the single cycle random simulation environment is normally used for all functional verification" (Page 3, Paragraph 0035)].**

As per claim 12, Hoppe et al. discloses, "wherein the jitter elements are interactively inserted by user." **["A verification engineer inputs a design specification to a behavioral checker. The behavioral checker typically comprises a general-purpose computer, which is equipped with software for the developing behaviorals from the specification into functional checker programs" (Page 2, Paragraph 0022)].**

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 9, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over B. W. Curran et al. ("IBM eServer z900 high-frequency microprocessor technology, circuits, and design methodology" July/September 2002, IBM Journal of Research and Development, VOL. 46, NO 4/5) and well know practices in the art.

As per claim 9, B.W. Curran et al. discloses, a logic synthesis method/process that uses a functional descriptive language "VHDL" (Page 638, Column 2) to implement the electronic circuit's function into digital logic gates "inverter, NAND2, NAND3, NOR2, etc." (Page 638, Column 1), and then performs timing verification/simulation (Page 638, Column 2) on the resulting logic implementation.

B.W. Curran et al. does not disclose expressly the limitation of a "cycle level" simulation in accordance with the applicants provided definitions of "In cycle level simulations logic functions effectively happen in zero time, so generally appear to change at the same time." (Page 2, Line 19).

However, at the time of the invention it would have been obvious to a person of ordinary skill in the art that the application of the method/process disclosed in B. W. Curran et al. leads to the usage and generation of a "cycle level" simulation prior to the timing verification/simulation phase of the method/process. It is obvious that during the logic synthesis phase of implementation of the functional description of the digital logic circuit "gate-mapping algorithms" (B.W. Curran et al. Page 638, Column 1) that logic verification of the design is also being conducted to verify that the implementation of the logic matches the functional description prior to performing the computational complex timing verification/simulation. It is additionally obvious that a "cycle level" verification/simulation would be conducted prior to the timing verification/simulation since timing verification/simulations require excessive amounts of memory space and CPU time to perform the complex computations, and these resources would otherwise

be wasted if performed on a design that was functionally inaccurate prior to timing analysis.

It is additionally obvious to one skilled in the art that a "cycle level" verification/simulation could also be conducted during the timing verification/simulation by increasing the clock period to a length of time that effectively would appear to the simulation to be infinite (i.e. changing the clock period from nanoseconds to seconds in a register transfer logic RTL design).

As per claim 11, B.W. Curran et al. discloses, the usage of a functional descriptive language ("VHDL" Page 628, Column 2) for usage in the synthesis method/process.

B.W. Curran et al. does not disclose expressly, the usage of exercising predetermined signals randomly into the design.

However, at the time of the invention it would have been obvious to one skilled in the art that predetermined signal values can be generated by appropriately declaring and implementing in the functional descriptive language the signals and/or input/output pins by tying the appropriate signals and/or input/output pins to either GND (logic level 0 or low voltage level) or VDD (logic level 1 or high voltage level). Additionally the control logic that would randomly activate the predetermined signal values is also appropriately declared and implemented in the functional descriptive language. Once appropriately declared and implemented in the functional descriptive language the design can be implemented using the method/process outlined in B.W. Curran et al. resulting in the timing verification/simulation of the design.

As per claim 12, B.W. Curran et al. discloses, the usage of a functional descriptive language ("VHDL" Page 628, Column 2) for usage in the synthesis method/process and also the process of automatically inserting "jitter elements" into the design as "early-mode problems were automatically fixed" (Page 639, Line 6).

B.W. Curran et al. does not disclose expressly the limitation of "jitter elements being interactively inserted by the user" (Claim 12, Line 1).

However, at the time of the invention it would have been obvious to one skilled in the art that the user can interactively insert "jitter elements" by appropriately declaring and implementing "jitter elements" in the functional descriptive language. The motivation for adding, "jitter elements" (increase timing delay) to the functional description is to delay the arrival of a signal to the destination logic to eliminate an early timing issue or race condition.

Conclusion

20. In addition to references used under 35 U.S.C. 102, additional prior art references that disclose relevant subject matter on the merits can be found in Schaumont et al. (US 7,006,960 B2) February 28, 2006 and "Cadence NC-Verilog Tutorial for SimVision Waveform Viewer Users" (Product Version 3.40, January 2002). Cadence NC-Verilog Tutorial Teaches:

a. Simulation of electronic circuits that can consist of asynchronous clock domains.

b. Allows for the insertion of additional logic in the simulation via the addition of functional code in the VHDL or by updating the schematic in the "Schematic Window".

c. Allows for the uploading/programming of simulation/signal values.

21. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan R. Plante whose telephone number is (571) 272-9780. The examiner can normally be reached on Monday through Friday 9:00 AM to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pierre M. Vital can be reached on (571) 272-4215. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 2, 2006
JRP

Jonathan Plante
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